REMARKS

Claims 1, 3, 5, 13, 24, 50, 62, and 73 have been amended. Claims 10, 22, 33, 59, 71, and 82 have been canceled. Claims 1-9, 11-21, 23-32, 34-58, 60-70, 72-81, and 83-98 are now pending. Claims 35-49 and 84-98 are withdrawn from consideration. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

A replacement sheet of drawings (FIGS. 6(a)-6(d)) is concurrently filed herewith. The replacement sheet labels FIGS. 6(a)-6(d) as "Prior Art." The Examiner approved of the proposed drawing corrections in the Office Action dated June 16, 2003.

Claims 1-9, 11-21, 23-32, 34, 50-58, 60-70, 72-81 and 83 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' "admitted prior art" in view of Ting and Washizuka. Reconsideration is respectfully requested.

Applicants' invention relates to a method of fabricating amorphous silicon thin film transistors without employing an etching process for the amorphous silicon thin film transistors layers. In particular, with the present invention, an etching step at the channel portion of the amorphous silicon layer (channel etching is illustrated in Fig. 6(c)) can be avoided. As a result, the thickness of the amorphous silicon layer can be reduced, and may be formed thinner than the silicon layer illustrated in AAPA and Washizuka. The channel etching process may remove the amorphous silicon layer completely when the amorphous silicon layer is thin.

To remove the channel etching step from the amorphous silicon thin film transistors fabrication process, the present invention puts phosphorous impurity 5 (illustrated in Fig. 1(a) on the surface of the amorphous silicon layer 4) without diffusing the impurity 5 into the amorphous silicon layer 4. The thickness of the phosphorous diffused layer is essentially zero prior to annealing. That is, essentially none of the impurity 5 is diffused into the amorphous silicon layer 4 prior to annealing. As a result, the

phosphorous impurity 5 can easily be removed from the surface of the non-doped amorphous silicon layer by exposing it to hydrogen plasma as illustrated in Fig. 1(c).

In contrast to the present invention, Ting uses the second doped amorphous silicon layers with a thickness of about 100 to 300 angstroms with phosphorous dopant (col. 2, lines 47-53). The thickness of Ting's doped amorphous silicon layers are almost the same as the low resistance amorphous silicon layer shown in Applicant's Fig. 6(a) (black circles within the white layer (65)) and the n+ (phosphorous) doped microcrystalline Si layer in Washizuka (pg. 208, left column, line 26). In these cited references, it would be difficult to remove the phosphorous dopant distributed inside these layers by hydrogen plasma.

In the cited prior art, an etching process must be used to remove the doped amorphous silicon with phosphorous impurity above the non-doped amorphous silicon layer without phosphorous impurity. In this case, the non-doped amorphous silicon layer without impurity would be partially removed at the same time during the etching process. Therefore, the thickness of the non-doped amorphous silicon layer without impurity cannot be reduced as that of the present invention.

After removing the phosphorous impurity just above the channel portion, the residual phosphorous dopant, protected from the hydrogen plasma, covered by the source drain electrodes, is diffused into the amorphous silicon layer by thermal annealing after the hydrogen plasma process to make the second amorphous silicon layer of lower resistance selectively under these electrodes. During this diffusing process, the resistance of the channel portion is not reduced because the phosphorous impurity is removed by hydrogen plasma. This is quite a different situation compared with Ting where the purpose is to reduce the resistance of amorphous silicon layer uniformly to make a gate electrode by distributing uniformly the phosphorous dopant by using the multilayer structure. (The phosphorous diffusing process referred to in Ting is described in textbooks such as "Physics and Technology of Semiconductor Devices" (Andrews S. Grove, John Wiley & Sons, Inc. 1967)).

An important difference between the present invention and the prior art of record is the thickness of the amorphous silicon layer with phosphorous dopant before hydrogen plasma and annealing. The thickness of any doped amorphous silicon layer is almost zero in the present invention (the dopant is located just on the surface of the amorphous silicon layer and is not yet diffused into the amorphous silicon); whereas in the cited references, this is a doped layer that is 100-300 angstroms thick.

Washizuka does not rectify the deficiencies associated with the other cited art. Washizuka is relied upon for etching the amorphous silicon layer utilizing a common photoresist to form the electrodes.

The cited prior art, even in combination, does not teach or suggest all of the limitations found in independent claims 1, 13 and 24. In particular, the art does not teach or suggest, "providing an impurity on the surface of said amorphous silicon layer," as recited in claim 1; "providing an impurity over said amorphous silicon layer, wherein said amorphous silicon layer does not contain said impurity," as recited in claim 13; or "providing an impurity on the surface of said amorphous silicon layer . . . wherein essentially none of said impurity is diffused into said contact portion prior to said removing step," as recited in claim 24.

Accordingly, withdrawal of the rejection of claims 1, 13 and 24 is solicited. Claims 2, 4 and 6-12 depend from claim 1, claims 14-23 depend from claim 13, and claims 25-34 depend from claim 24. Independent claims 3 and 5 include all of the limitations of independent claim 1. All of these claims are allowable for at least the reasons set forth above with respect to their independent claims 1, 13 and 24.

In addition, the Office Action does not comply with 35 U.S.C. § 103(a), in that it fails to explain how the thickness of the amorphous silicon layer, the concentration of impurity, and the exposure time as recited in dependent claims 2, 4, 8, 14, 16, 20, 25, 27 and 29 are rendered obvious. Indeed, the Office Action acknowledges that the Applicants' admitted prior art "fails to teach the thickness of the amorphous silicon film, the

concentration of the impurity, and the exposure time as recited." (Office Action, pg. 4).

Independent claims 50, 62 and 73 should be allowable for reasons similar to those discussed above. Claims 51-61 depend from claim 50, claims 63-72 depend from claim 62, and claims 74-83 depend from claim 73. All of these claims are allowable for at least the reasons set forth above.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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